REMARKS/ARGUMENTS

Claims 1-11 are pending in the application; the status of the claims is as follows:

Claims 1-5 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,448,655 to Yamaguchi ("Yamaguchi").

Claims 6-11 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamaguchi, and further in view of U.S. Patent No. 5,117,468 to Hino et al ("Hino et al").

The acknowledgement, in the Office Action, of a claim for foreign priority under 35 U.S.C. § 119(a)-(d), and that the certified copy of the priority document has been received, is noted with appreciation.

The indication, in the Office Action, that the Examiner has no objections to the drawings filed on November 12, 1999, is noted with appreciation.

Claims 1, 6, 8, and 11 have been amended to more particularly point out and distinctly claim the invention and claims 12 and 13 have been added. These changes do not introduce any new matter.

35 U.S.C. § 102(b) Rejection

The rejection of claims 1-5 under 35 U.S.C. § 102(b) as being anticipated by Yamaguchi, is respectfully traversed, because Yamaguchi fails to disclose each and every limitation recited in the subject claims. Specifically, Yamaguchi fails to disclose an address memory that stores the relative position within an image of a portion of the image data being processed by each of a plurality of processors. Such a structure is required by the claims. For example, claim 1 recites:

> "an address memory storing address information related to a position of each portion of said input image data within said input image

data for each respective portion of image data being processed by said plurality of processors."

Yamaguchi appears to disclose an image processor, wherein each processor computes a physical memory address in a random access memory, *e.g.*, RAM, for each pixel being processed by the processor based on its assigned allocation ratio. *See* column 3, lines 30-56. Because of this arrangement, the address of the n-th pixel of an image depends on where in the RAM the image is stored.

In contrast, the apparatus of claim 1 includes an address memory for storing a relative position of the image data, *e.g.*, pixel, within the whole image. Thus, the address of the n-th pixel of an image always has the same relative address within the image. This facilitates reassembly of the image data portions into a final image without the need to determine an offset from a starting address in a RAM memory. It is respectfully submitted that Yamaguchi does not disclose the claimed address memory and therefore does not read on claim 1.

With respect to claims 2-5, these claims depend from claim 1 and therefore distinguish Yamaguchi for at least the same reasons as applied to claim 1 above. Moreover, claim 2 further distinguishes Yamagughi, because the later fails to disclose "read means reading said image data from said image memory on the basis of said address information stored in said address memory." This feature of claim 2 requires that the read means retrieves *output* image data from the image memory based on the information in the address memory. At most, Yamaguchi discloses a plurality of processors that write image data to an image memory based on a calculated RAM memory address. Thus, Yamaguchi does not disclose an analogous structure. Accordingly, claim 2 distinguishes and is allowable over Yamaguchi.

Regarding the rejection of claim 4, it is respectfully submitted that column 3, line 12-16 and lines 17-29, do not disclose that input and output processing are performed in synchrony with an external device as stated in the Office Action. Rather, the cited

passages merely state that "the data processing abilities of the unit processors A11, B12, C13 are the same," and that the unit processor A11 has an additional burden because it has additional jobs such as controlling a scanner or hard drive.

Accordingly, it is respectfully requested that the rejection of claims 1-5 under 35 U.S.C. § 102(b) as being anticipated by Yamaguchi, be reconsidered and withdrawn.

35 U.S.C. § 103(a) Rejection

The rejection of claims 6-11 under 35 U.S.C. § 103(a), as being unpatentable over Yamaguchi, and further in view of Hino et al, is respectfully traversed because the references are not properly combinable, and because the combination fails to disclose the features of claims 6-11.

If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. MPEP 2143.01. Yamaguchi teaches using multiple processing units that share access to an image memory and process portions of an image stored in the image memory subject to a calculated allotment ratio. *See* Figs. 4 and 5, and column 2, lines 57-69 and column 3, lines 43-56. The processors operate independently, so that, for example, unit processor A11 may also provide Input/Output processing to a scanner or hard drive. In contrast, Hino teaches a plurality of shift registers that feed pixel data to local image processing circuits in a fixed sequence and in lock step synchronization. It is therefore entirely unfathomable how the two references may be combined without significantly altering the principle of operation of one or both of the references. Accordingly, it is respectfully submitted that it is improper to combine the references as suggested.

Furthermore, assuming *arguendo* that the combination were proper, the combination still fails to teach every feature of the subject claims. Specifically, the combination fails to teach or suggest, a first memory in which is stored arrangement

information for each divided data being processed as required by claim 6. Yamaguchi teaches calculating a RAM memory address based on an allotment ratio. Hino teaches relatively complex circuitry including DMA controllers, counters, shift registers, parallel/serial converters, and the like, operative to transfer pixel data from a RAM address to the local image processors and then store processed pixels at another RAM address. It is therefore respectfully submitted that the combination does not read on either claim 6, or claims 7-10 which depend therefrom.

In regards to claim 11, it is respectfully submitted that the combination of Yamaguchi and Hino is improper for the reasons given above. Moreover, even if the combination were proper, the combination still fails to teach or suggest an image processing method including steps of "storing address information" and "outputting said processed data as well as said address information" as required by claim 11.

Accordingly, it is respectfully requested that the rejection of claims 6-11 under 35 U.S.C. § 103(a) as being unpatentable over Yamaguchi, and further in view of Hino et al, be reconsidered and withdrawn.

New Claims

It is respectfully submitted that new claims 12 and 13 distinguish the cited art because the cited art fails to teach, suggest, or otherwise disclose an image processor including multiple processors having separate ports for inputting image data and image address data for outputting processed image data and image address data. Accordingly, claims 12 and 13 are allowable over the art of record.

CONCLUSION

Wherefore, in view of the foregoing amendments and remarks, this application is considered to be in condition for allowance, and an early reconsideration and a Notice of Allowance are earnestly solicited.

This Amendment increases the number of independent claims by 1 from 3 to 4 and increases the total number of claims by 2 from 11 to 13, but does not present any multiple dependency claims. Accordingly, a Response Transmittal and Fee Authorization form authorizing the amount of $86.00 to be charged to Sidley Austin Brown & Wood LLP's Deposit Account No. 18-1260 is enclosed herewith in duplicate. However, if the Response Transmittal and Fee Authorization form is missing, insufficient, or otherwise inadequate, or if a fee, other than the issue fee, is required during the pendency of this application, please charge such fee to Sidley Austin Brown & Wood LLP's Deposit Account No. 18-1260.

Any fee required by this document other than the issue fee, and not submitted herewith should be charged to Sidley Austin Brown & Wood LLP's Deposit Account No. 18-1260. Any refund should be credited to the same account.

If an extension of time is required to enable this document to be timely filed and there is no separate Petition for Extension of Time filed herewith, this document is to be construed as also constituting a Petition for Extension of Time Under 37 C.F.R. § 1.136(a) for a period of time sufficient to enable this document to be timely filed.

Any other fee required for such Petition for Extension of Time and any other fee required by this document pursuant to 37 C.F.R. §§ 1.16 and 1.17, other than the issue fee,

and not submitted herewith should be charged to Sidley Austin Brown & Wood LLP's Deposit Account No. 18-1260. Any refund should be credited to the same account.

Respectfully submitted,

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April 21, 2004

DA1 286577v4